REMARKS

The application has been amended, and is believed to have been placed in condition for allowance. This amendment is submitted as part of a Request for Continued Examination (RCE).

Amendments to the Application

Claim 1 is amended to incorporate the recitations of dependent claims 2 and 4. Claims 2 and 4 are canceled without prejudice. Amended claim 1 finds support in the specification and the drawing figures as originally filed (e.g., paragraphs [0029] and [0031]).

Claim 8 is amended to incorporate the recitations of dependent claims 9 and 11. Claims 9 and 11 are canceled without prejudice. Amended claim 1 finds support in the specification and the drawing figures as originally filed (e.g., paragraphs [0029] and [0031]).

Claim 17 is amended corresponding to the amendments to claims 1 and 8, and finds support in the specification and the drawing figures as originally filed (e.g., paragraphs [0029] and [0031]).

The amendments to the claims do not introduce new matter.

Formal Matters - Objections to the Claims

The Official Action objected to claim 1 based on informalities.

In reply, claim 1 has been amended responsive to the Official Action's objection. Withdrawal of the objection is respectfully solicited.

Formal Matters - Rejections under Section 112

The Official Action rejected claims 1-7 and 15 under 35 USC 112, first paragraph, stating that the claims contain subject matter not described in the specification in such a way as to reasonably convey to one of skill that the inventors had possession of the claimed invention.

In particular, the Official Action states as to claim 1 that the recitation "reducing risks of delays in the directionally transfer of data packets through the pipeline" does not appear to be disclosed in the original disclosure.

In reply, objected recitation is deleted from claim 1.

Withdrawal of the rejection under section 112, first paragraph is respectfully solicited.

The Official Action rejected claims 17-20 under 35 USC 112, second paragraph as being indefinite based on insufficient antecedent basis for a recitation of claim 17.

In reply, claim 17 has been amended to overcome the Official Action's rejection. Withdrawal of the rejection under section 112, second paragraph is respectfully requested.

Substantive Matters - Section 103

The Official Action rejected claims 1-16 and 19-20 under 35 USC 103(a) as being unpatentable over CATALDO ("Net Processor Startup Takes Pipelined Path to 40 Gbits/s") in view of DORST (U.S. Pub. 2004/0098549 A1) and further in view of HARRIMAN (U.S. Patent 6,330,645).

The Official Action rejected claim 17 under 35 USC 103(a) as being unpatentable over CATALDO in view of DORST.

The Official Action rejected claim 18 under 35 USC 103(a) as being unpatentable over CATALDO and DORST, and further in view of BERGGREEN (US Pub. 2003/0016685).

The rejections are respectfully traversed for at least the reasons that follow.

It is firstly noted that independent claims 1, 8 and 17 are amended, as indicated above.

It is respectfully submitted that the cited references, either individually or in combination, fail to teach or suggest the invention recited in claims 1, 8 and 17 as amended.

As specified in the amended claims, the present invention differs from the cited prior art in that the claimed interface engine comprises a microcode memory (230), and is configured to:

- receive a request (170) from the pipeline upon arrival of a data packet at any one of the connected access

points, the request comprising a first request code (210), according to a first coding scheme adapted for the processor,

- execute a microcode program stored in the microcode memory (230), the execution of the microcode program being dependent upon the first request code, to obtain, as a result of the execution of the microcode program, at least one device control code (300) according to a second coding scheme adapted for the external device (140), wherein the execution of the microcode program being dependent upon the first request code in that the start address of the microcode program corresponds at least partly to the first request code,

- generate at least one request output (270, 290), the at least one request output being based at least partly on the request (170) from the one access point and/or at least partly on the device control code (300), and

- send the at least one request output (270, 290) to the external device (140).

The reference numerals in parentheses are provided to illustrate an embodiment of the invention as disclosed in the present application for the Examiner's convenience.

I. DORST FAILS TO TEACH OR SUGGEST A REQUEST COMPRISING A FIRST REQUEST CODE

The Official Action states that DORST discloses that "the request comprises a first request code according to a first coding scheme". The Official Action further states that it is

"inherent that a data instruction such as a load or a store has parameter bits to indicate the address or memory module that needs to be accessed; these bits correlate to the request code and its format to be recognized is the coding scheme."

Applicants respectfully disagree. In DORST, the data instruction comprises information about the external device (memory 1, 1015A to memory N, 1015N) that needs to be accessed, and a format for the instruction being adapted for the external device (see, e.g., paragraphs [0029], [0046]).

As specified in the amended independent claims, the request comprises a first request code according to a first coding scheme adapted for the processor. Thus, the first request code of the present invention relates to the pipeline from which the request is sent and not to an external device to be accessed as described in DORST.

Further, as specified in the amended independent claims, at least a part of the first request code corresponds to a start address of the microcode program to be executed by the interface engine, the microcode program being stored in a microcode memory of the interface engine. Thus, a part of the first request code corresponds to an address of the internal microcode memory, contrary to the position of the Official Action regarding the data instruction of DORST, wherein the data instruction of DORST comprises information about an external device to be accessed.

II. DORST FAILS TO TEACH OR SUGGEST AN INTERFACE ENGINE ADAPTED TO EXECUTE A MICROCODE PROGRAM

The Official Action also contends that DORST discloses an "interface engine being adapted to execute a program", stating that DORST [0070] and [0071] discloses "using finite state machines, counters and programmable registers in order to implement the control circuitry for the memory controller and establish relative timing relationships among control signals and address signals, which is in effect executing a program".

On the contrary, the memory controller 1005 of DORST is realized by hardware only. As stated in paragraphs [0070] and [0071], "the memory controller 1005 includes finite state machines, counters and glue logic circuitry (...) that implement control circuitry for the memory controller 1005". Consequently, once the control circuitry of the memory controller 1005 of DORST has been created on an integrated circuit it cannot easily be re-adjusted to new external devices connected to the memory controller without disassembling the memory controller and control circuitry. DORST makes no disclosure that its finite state machines, counters, and glue logic circuitry have any structure other than that of a hard-wired machine. That is, there is no teaching or suggestion in DORST that the memory controller 1005 comprises a microcode memory, means for processing microcode, and supporting structure for the loading and execution.

In contrast, the amended independent claims require the interface engine to comprise a microcode memory, and configured to execute a microcode program. This requirement of the amended independent claims is fundamentally different from the operation of a finite state machine, which does not teach the execution of a microcode program.

It is well understood in the art that a finite state machine is a model of behavior composed of a finite number of states, transitions between those states, and actions (see, e.g., http://en.wikipedia.org/wiki/Finite_state_machine). In a digital circuit, an finite state machine may be built using a programmable logic device, a programmable logic controller, logic gates and flip flops or even mechanical relays (see, *id.*). More specifically, a hardware implementation requires only a register to store state variables, a block of combinational logic which determines the state transition, and a second block of combinational logic that determines the output of a finite state machine (*id.*).

Hence, a finite state machine, such as that disclosed by DORST, does not inherently disclose microcode, microcode execution, microcode memory, or a microcode program stored therein (see, e.g,. http://en.wikipedia.org/wiki/Microcode: "Microcode is a layer of lowest-level instructions involved in the implementation of machine code instructions in many computers and other processors; it resides in a special high-speed memory

and translates machine instructions into sequences of detailed circuit-level operations... it helps separate the machine instructions from the underlying electronics so that instructions can be designed and altered more freely.")

III. DORST FAILS TO TEACH OR SUGGEST EXECUTION OF A MICROCODE PROGRAM DEPENDENT UPON A FIRST REQUEST CODE

The Official Action contends that DORST discloses "the execution being dependent upon the first request code", stating that DORST at paragraph [0071] discloses that programmable registers provide a mechanism for timing among control signals, and that paragraph [0039] specifically discloses that the programmable registers store read timing-parameters and write timing-parameters. Furthermore, the Official Action states that "Because [0042] discloses that each memory may correspond to a respective register set, it is inherent that, once a memory instruction occurs and its relevant parameters are sent to the memory controller, the bits regarding the specific address or memory to be accessed are used in some form to select the register with the timing-parameters relevant to that specific address or memory. These timing-parameters are used by the finite state machine to execute the program, as certain control signals are asserted at certain times to certain memory because of the parameters/code of the memory instruction".

Applicants respectfully disagree. As stated above, the finite state machine of DORST does not teach or suggest executing

a microcode program as described by the present invention, and therefore does not disclose an interface engine adapted to execute a microcode program stored in the microcode memory, the execution being dependent upon the first request code, the first request code being according to a first coding scheme adapted for the processor and corresponding at least partly to a start address of the microcode program. DORST provides neither teaching nor suggestion of this.

IV. DORST FAILS TO TEACH OR SUGGEST EXECUTING A MICROCODE PROGRAM TO OBTAIN AT LEAST ONE DEVICE CONTROL CODE

The Official Action contends that DORST discloses "to obtain, as a result of the execution of the program, at least one device control code, according to a second coding scheme", stating that DORST "succinctly states in the third sentence of the abstract, the interface circuitry communicates with the memory by providing a plurality of control signals; as explained above, certain controls signals, correlating to device control code, are asserted at certain times as a result of executing the finite state machine that correlates to the memory being accessed. This second coding scheme is the code that is outputted to the memory which controls the memory, as opposed to the first coding scheme which is the code that makes up the instruction."

Applicants respectfully disagree. As stated above, the finite state machine of DORST does not teach or suggest executing a microcode program as described by the present invention. Thus,

a control signal 4025 to the memory 1015 is not obtained as a result of an execution of a program.

V. RECONSIDERATION IS REQUESTED

Based on the reasons set forth above, it is respectfully submitted that none of the cited references, individually or in combination, teach or suggest all the features recited in the amended independent claims.

Reconsideration and withdrawal of the rejections under section 103 are respectfully requested.

From the foregoing, it will be apparent that Applicants have fully responded to the November 19, 2008 Official Action and that the claims as presented are patentable. In view of this, Applicants respectfully request reconsideration of the claims, as presented, and their early passage to issue.

In order to expedite the prosecution of this case, it is requested that the Examiner telephone the attorney for Applicants at the number set forth below if the Examiner is of the opinion that further discussion of this case would be helpful.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any

overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

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